

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL NO:

In Re Application of:
Peter I. A. Barri, et al.

Dated: December 7, 2006

Serial No.: 09/990,840

Group Art Unit: 2187

Filed: 11/21/2001

Examiner: Peugh, Brian R.

For: SYSTEM AND METHOD OF MAINTAINING HIGH BANDWIDTH
REQUIREMENT OF A DATA PIPE FROM LOW BANDWIDTH MEMORIES

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTIFICATION OF NON COMPLIANT APPEAL BRIEF

Sir:

In Response to the Notification of Non-Compliant Appeal Brief mailed on 12/01/2006, submitted herewith is the corrected Appeal Brief including the “Related Proceeding Appendix”, the alleged missing part.

The Commissioner is hereby authorized to charge any fees or credit any overpayment associated with this communication to deposit account 09-1990. If any unresolved issues remain please contact applicant’s attorney at 919-543-9036.

APPELLANT'S BRIEF ON APPEAL

I. REAL PARTY IN INTEREST

The real parties in interest are Assignees Alcatel and International Business Machines Corporation (IBM).

II. RELATED APPEALS AND INTERFERENCES

Appellants or Appellants' legal representative or assignees have no personal knowledge of other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-4, 24-27, 33, and 34 are on appeal. This application, as originally filed, included Claims 1-28. By Examiner's restriction, Claims 10-22 were deemed drawn to distinct invention and are withdrawn.

Claims 29-34 were added by amendment. The Examiner unilaterally withdrew Claims 29-32. Claims 35-36, added by amendment, are objected to.

Claims 5-9 and 28 are allowed and not part of this appeal.

IV. STATUS OF AMENDMENTS

Subsequent to the Final Rejection, an amendment canceling Claim 36 is filed concurrently with this appeal brief.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides a system (memory) and method that allow relatively slow but dense (stores large amounts of data) storage components, such as DDR DRAM, supply data to high speed channel termed "FAT Pipe", Fig. 1, 22 and pg. 10, lines 3-5. DDR DRAMs are relatively low cost and have the capacity to store large amounts of data. But they are slow and prior to this invention could not be used in this environment.

Claim 1 recites N different memories... (page 10, lines 5-7, page 9, lines 9-11, page 14, lines 14-17, and Figs. 2 and 3, elements labeled Slice O-N); M different busses (page 14, lines 15-16, pages 19-20, lines 18-21 and lines 1-2, Fig. 4, O'-N')...each having bandwidth to transport data at a predetermined rate (page 23, line 15, Fig. 6, 7.75, 15.5, etc. and page 15, lines 1-5, Fig. 5, 7.75 Gbps); a plurality of different memory controllers (page 9, lines 10 and 15, Fig. 2, DRAM Ctrl 0 – DRAM Ctrl N)...each one of the plurality of memory controllers setting associated different memory in at least a first mode (page 3, lines 1-6); a single arbiter (Page 12, lines 17-20, page 13, lines 2-14, Figs. 2 and 3, 24 and 36) responsive to at least one signal requesting access (page 19, lines 18-20, Fig. 2, W Request and R Request) to the N different memories wherein said single arbiter generate an Access Vector (Fig. 3, 24 and 36) that causes information to be read simultaneously (page 15, lines 1-18) from multiple ones of the N different memories...wherein total bandwidth on selected ones of the M busses...is greater than bandwidth on a single bus... (Page 3, lines 7-15).

Dependent Claim 3 calls for...the N different memories includes DDR DRAM (page 14, line 15, Fig. 2, Slice 0 – Slice N).

Dependent Claim 4 recites...DDR DRAM partitioned into at least four banks and at least one buffer is spread across the at least four banks (page 20, lines 5-10, Fig. 4, O' – N', Fig. 5, shaded area in Slice 0-Slice N, labeled buffer spread over 4 banks).

Independent Claim 24 recites: a method comprising providing a plurality of separate memory elements in which frames from a communication device are to be stored or retrieved (page 9, lines 10-20, page 13, lines 15-17, Fig. 2, Slice 0 – Slice N, 26, and 30); partitioning the frame with a controller into at least two parts (page 11, lines 15-18, Fig. 2, receive controller 26, page 21, lines 8-14); storing at least one of the at least two parts into different ones of the plurality of separate memory elements (page 21, lines 8-14); providing a single arbiter responsive to a request signal to cause the different ones of the plurality of separate memory elements to be read simultaneously wherein each one of the adjoining parts is available simultaneously on respective busses associated with each of said ones of the plurality of separate memory elements.

Simultaneous reading of memory is described at page 23, lines 2-15 and shown graphically in Fig. 6 by numbers 2 and 3. Numerals 40-50 represent memory cycles. During memory cycle 42, slice 4 and 3 are read simultaneously, yielding buffers 2 and 3. Likewise,

during access window 46, slice 0 and slice 3 are read simultaneously yielding buffers 5 and 6 (page 23, line 9). The single arbiter 24 (Figs. 2 and 3) responding to Read Request from transmit controller 30 (page 13, line 17) access multiple slices of memory simultaneously (page 15, lines 3-5).

Independent Claim 25, a method, recites: providing a plurality of separate memories in which data is stored; (Figs. 2 and 3, Slice 0 – Slice N, page 10, lines 5-7), Receive Control 26 (Fig. 3) receives data and writes the data into separate memories labeled Slice 0 – Slice 5, page 13, lines 15-17 Slice 0 – Slice N are memories in which data is stored) providing a single arbiter to grant access to the plurality of separate memories; (Memory arbiter 24 (Figs. 2 and 3) provides access to memory store Slice 0 through Slice N, page 12, lines 17 and 18) receiving in the single arbiter a request to read data from selected ones of said plurality of separate memories; The transmit controller 30 (Figs. 2 and 3) issues Read Request to the single arbiter 24 to read data from selected memories, page 15, line 12. The single arbiter 24 controls access to memory, page 15, lines 8-9) simultaneously reading said selected ones of said plurality of separate memories to provide data simultaneously on individual busses coupled to the selected ones of said plurality of separate memories. (As stated at page 15, lines 12-13, multiple slices (of memory) can be read at the same time simultaneously, Figs. 6, 2 and 3, pages 7-8.

Dependent Claim 26 recites...bandwidth of data on each one of the individual busses is less than the total bandwidth of all activated busses. (Page 3, lines 10-15, page 23, lines 11-15, Fig. 6).

Independent Claim 27 recites a method of writing parts of a frame over multiple memory modules and reading sufficient data from multiple memories to satisfy the requirement of a FAT pipe. (Page 3, lines 1-15 and page 10, lines 3-8). Claims 27 calls for: providing a plurality of separate memory modules in which frames are being stored; (Figs. 2 and 3 show plurality of memory modules labeled Slice 0 (DDR DRAM) through Slice N (DDR DRAM), page 9, lines 9-10) partitioning a frame into multiple parts; (Receiver Controller 26 (Figs. 2 and 3) receive frame, request free buffer addresses in the DDR DRAM and writes frame in the different memory address in separate DDR DRAM, Page 11, lines 15-18. Writing the frame in different memory addresses indicates partitioning, page 11, lines 15-18, page 15, lines 14-18, and page 18, lines 8-18) writing adjacent parts of the frame so partitioned in different ones of the plurality of separate memory modules; (adjacent parts of same frame are written in different memory slices,

page 15, lines 14-18) simultaneously accessing, with a single arbiter, multiple ones of the plurality of separate memory modules in a single memory access window to read data therefrom wherein the total bandwidth of data output from the multiple memory modules matches the bandwidth of a FAT pipe port associated with a communication device. (The memory arbiter 24 (Figs. 2 and 3) control access to memory slices, page 15, lines 8-9. A read request to arbiter 24 from transmit controller 30 (Figs. 2 and 3) can be executed at the same time simultaneously, page 15, lines 12-13. Fig. 6 shows graphical representation of frame being read from memory with buffers 2 and 3 being read simultaneously during access window 42 from slice 3 and slice 4, page 22, lines 18-19 and page 23, lines 7-10.

Independent Claim 33 recites a system comprising: N different memory elements, $N > 1$, wherein at least two of said N different memory elements are each partitioned into multiple sectors and each of the at least two of said N different memory elements so partitioned is partitioned into at least one buffer spread across multiple sectors; (Fig. 5 shows N memory elements 4 DDR DRAMs labeled slice 0 – slice N with each DDR DRAMs partitioned into sectors labeled A-D and each sector has buffer (shaded area) spread over multiple sectors) a plurality of memory controllers with each one of said plurality of memory controllers operatively coupled to each one of the N different memory elements; (Fig. 2 shows DRAM controller (cntrl) labeled 0- N connected by individual bus to N different memory elements labeled Slice 0 (DDR DRAM) to Slice N (DDR DRAM), page 9, line 15) a single arbiter operatively coupled to the plurality of memory controllers, said single arbiter being response to a write request signal to generate a write control signal that causes data to be written in one of the at least one buffer associated with one of the at least two of said N different memory elements. (Fig. 2 shows memory arbiter 24 couple to plurality of DRAM cntrl labeled 0- N and write (W) request extending from Receive Controller 26. In response to the W request the arbiter 24 issue access vector 36 (Fig. 3) that causes data to be written in memory, page 10, lines 3-10, page 11, lines 15-18, and page 13, lines 2-5.

Dependent Claim 34, relating to interleaving in which data is written into one memory and read from another, recites the single arbiter response to read request signal generate a read control signal that causes data to be read from another of the at least one buffer associated with another of the at least two of said N different memory element.

As stated relative to Claim 33 above, Figs. 2 and 3 show single arbiter 24 accepting W request from Receiver Controller 26, R request from transmit controller 30 and generate access vector 36 to R/W data from/into memory, as the case may be, page 13, lines 2-4 and page 15, lines 12-13. Fig. 6 demonstrates interleaving in which the buffer labeled 1 is being read from Slice 1 and the buffer labeled A is written in Slice 2, page 23, lines 5-6, and page 23, lines 16-17.

VI. GROUPING OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether the Declaration Under 37 CFR 1.132 filed by co-inventors of the appealed claims is sufficient to establish inventorship and remove U.S. Patent 6,460,120 B1 (Bass et al.) as reference.

B. Whether Claims 1-4, 25, 26, 33, and 34 are anticipated under 35 USC 102(e) by U.S. Patent 6,460,120 B1 (Bass et al.).

C. Whether Claim 24 is patentable, under 35 USC 103(a), over U.S. Patent 6,560,227 (Bartoldus et al.) in view of U.S. Patent 6,460,120 (Bass et al.)

D. Whether claim 27 is patentable, under 35 USC 103(a), over U.S. Patent 6,560,227 (Bartoldus et al.) in view of U. S. Patent 6,460,120 (Bass et al.) and Applicants' Admitted Prior Art.

VII. ARGUMENTS

Arguments traversing each of the rejections set forth in VI will be identified with like alphabetical characters.

A. Declarations submitted pursuant to 37 CFR 1.132 are sufficient to establish inventorship and remove U.S. Patent 6,460,120 B1 as reference.

Claims 1-4, 24-26, 33 and 34 (claims on appeal) are rejected based upon U.S. Patent 6,460,120 B1 (Bass et al.).

In the Final Office Action mailed 06/16/2004 (Paper #11), the Examiner in part states that rejection based upon U.S. Patent 6,460,120 (applied reference) might be overcome by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention by another.

Because the rejection was final, Appellants filed a RCE and introduced into evidence the Declaration Under 37 CFR 1.132. A copy of the Declaration is provided in Evidence Appendix. The Examiner is of the opinion that the Declaration is insufficient and support his position by argument set forth on pages 13-15 of the Office Action mailed 12/08/2004.

A(1). APPELLANTS' CONTENTION

It is appellants' contention the Declaration meets requirements set forth by the court and the Patent Office. As a consequence, it is sufficient and the reference U.S. Patent 6,460,120 B1 (Bass et al.) should be withdrawn.

MPEP 716.10 (Rev. 1. Feb. 2003, pg. 700-250) states: "An uncontradicted 'unequivocal statement' from the applicant regarding the subject matter disclosed in an article, patent or published application will be accepted as establishing inventorship." In re DeBaun, 687 F.2d 459, 214 USPQ 933, 936 (CCPA 1982). A copy of pg. 700-250 MPEP is included in the Evidence Appendix.

Declarations were submitted by each of the co-inventors of the present invention. The contents of the Declarations are identical. Appellants assert paragraphs 2 and 3 of the Declaration unequivocally states appellants are the inventors of subject matter disclosed but not claim in U.S Patent 6,460,120 B1 (Bass). There is no evidence in the record to contradict this unequivocal assertion of inventorship. Therefore, the Declaration falls clearly within the above guideline promulgated by the Patent Office and the Court. As a consequence, the Declaration of Appellant should be sufficient, without further showing, to remove this patent as reference against the invention as claimed.

It seems the argument of the Examiner requiring further proof or showing to establish inventorship has gone far beyond and appears incongruous with the guidelines promulgated by the Patent Office and Courts. As a consequence, Appellants' move the Board to find the Declaration sufficient and reverse the Examiner. In case such a finding is made, the appeal claims are allowable and the remaining parts of this brief are irrelevant.

B. Claims 1-4, 25, 26, 33, and 34 Not Anticipated by U.S. Patent 6,460,120 (Bass et al.)

Claims 1-4, 25, 26, 33, and 34 are rejected under 35 USC 102(e) as being anticipated by U.S. Patent 6,460,120 (Bass et al.). For reasons set forth herein, Appellants contend the claims are not anticipated.

B(1). Law As Applied to Rejection Under 35 USC 102 (Anticipation)

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in...the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

B(2). Rejection of Claims 1-2

Appellants contend Claims 1-2 are patentably distinguishable from U.S. patent 6,460,120 B1 (Bass et al.). Claim 1 calls for a single arbiter responsive to...signal requesting access to the N different memories wherein said single arbiter generates an access vector that causes the functions recited in Claim 1.

Neither the teaching of a single arbiter nor the function it provides according to Claim 1, is found in U.S. Patent 6,460,120 B1. Instead, the subject patent (hereinafter Bass et al.) teaches a memory subsystem having multiple memory chips with each one being connected to a different arbiter. Fig. 13, Col. 24, lines 41-44.

It is Appellants' contention the structure set forth in Bass et al. fails to teach the single arbiter performing functions as claimed in Claim 1. Therefore, under the law of anticipation, set forth above, Claim 1 is not anticipated by Bass et al.

Claim 2 depends on Claim 1 and is patentable over Bass et al. due to its dependency incorporating the limitation from Claim 1.

The argument of the Examiner set forth on page 4 of the Final Office Action mailed 8/24/2005 appears to be in error. Because the structure of the memory and its description as disclosed in Bass et al. could not be reasonably construed to teach a single arbiter having access

to multiple memories....causing simultaneously reading of multiple ones...wherein total bandwidth exceeds bandwidth on single bus.

In fact, the Examiner admits in the argument on page 4 of the Final Office Action that Bass et al. does not specifically recite bandwidth in terms of the busses and memories. The Examiner seems to rely on inherency to meet this feature of the claim. But Appellants assert inherency is not applicable and the admission should be construed as evidence of novelty over Bass et al.

B(3). Rejection of Claim 3

Claim 3 is patentable due to dependency on Claim 1.

In addition, it is separately patentable in that it calls for DDR DRAMs control by a single arbiter whereas Bass et al. teaches a different structure (DDR DRAMs, each control by separate arbiter).

B(4). Rejection of Claim 4

Claim 4 is patentable over Bass et al. due to dependency on Claim 1. The argument set forth above is equally applicable and incorporated herein by reference.

In addition, Claim 4 is separately patentable. Claim 4 calls for "...each of the DDR DRAM is partitioned into at least four banks and at least one buffer is spread across the at least four banks." Appellants contend Bass et al. does not teach or suggest...at least one buffer spread across the at least four banks. As a consequence, Claim 4 is not anticipated by Bass et al.

In support of the rejection of Claim 4, the argument at page 5 of the Final Office Action mailed 8/24/2005 states: "Regarding Claim 4, Bass et al teaches partitioning the memory into at least four banks with a buffer spread across the four banks". (Col. 9, lines 55-60).

Appellants have reviewed Bass et al. including Col. 9, lines 51-60, and did not find any teachings or suggestion of spreading a buffer over four banks of the same DDR DRAM as set forth in Claim 4. The teachings at Col. 9, lines 51-60 (Bass et al.) seem to cover placing frame in one or two buffers formed from DDR DRAM, but no teaching of spreading a buffer across four banks of the same DDR DRAM. The conclusion of the Examiner that this feature of Claim 4 is disclosed or suggested in Bass et al. appears to be in error.

B(5). Rejection of Claim 25

Claim 25 recites the following elements, not found in Bass et al.:

- (a) Providing a single arbiter to grant access to the plurality of separate memories;
- (b) Receiving in the single arbiter a request to read data from selected ones of said plurality of separate memories; and
- (c) Simultaneously reading said selected ones of said plurality of separate memories to provide data simultaneously on individual busses coupled to the selected ones of said plurality of separate memories.

None of the above features were found or suggested in Bass et al. As a consequence, Claim 25 is not anticipated.

The arguments of the Examiner on page 5 of the Final Office Action (mailed 8/24/2005) which seem to suggest Bass et al. teaches providing a single arbiter to do what is recited in Claim 25 and simultaneously reading memories appears to be in error. For example, Bass et al., Col. 24, line 55, states: "Each Memory Arbiter contains...." This teaching clearly suggests multi-memory arbiter and not a single one as this claim recites.

B(6). Rejection of Claim 26

Claim 26 depends on Claim 25 and is patentable by reason of dependency. The arguments for patentability set forth in B(5) is equally applicable and is incorporated herein by reference. In addition, Claim 26 is separately patentable. Claim 26 recites: "...the bandwidth of data on each of the individual busses is less than total bandwidth of all activated bus."

It is Appellants' contention no such teaching is found in Bass et al. Therefore, Claim 26 is not anticipated.

As to Claim 26, the Examiner seems to admit it is not found in Bass et al. in the Final Office Action mailed 8/24/2005 (page 5, last paragraph). At page 6, line 1-3 (same Final Office Action), the Examiner states: "Since Bass et al. also teaches that multiple memories may be read from simultaneously, the multiple pieces of data will be read over the multiple busses at the same time."

Appellants contend the Examiner's position that Bass et al. teaches multiple memories may be read simultaneously appear to be in error. No such teachings could be found in Bass et

al. Therefore, the admission by the Examiner should indicate non-anticipation of Claim 26 by Bass et al.

B(7). Rejection of Claim 33

Claim 33 calls for (a) at least two memories partitioned in multiple sectors and buffer spread across the multiple sectors of each memory and (b) single arbiter...being responsive to write request to generate write control signal causing data to be written in one of the buffers."

It is argued in B(4) and B(2) above and incorporated herein by reference neither the spreading of buffer across multiple sector of a multi-sectored memory element nor a single arbiter performing write function in the buffer is disclosed or suggested in Bass et al. Therefore, Claim 33 is not anticipated by Bass et al.

B(8). Rejection of Claim 34

Claim 34 depends on Claim 33 and is not anticipated by Bass et al. for reasons set forth in B(7) and incorporated herein by reference.

Claim 34 is separately patentable. Claim 34 calls for the single arbiter responding to read request to generate a read control signal which causes data to be read from another of the two buffers located in another one of the N memory. In essence, Claim 34 requires a single arbiter causing spread buffer to be written in one memory and spread buffer to be read from another memory. No such feature is present in Bass et al. In Bass et al., each memory has a dedicated arbiter which cannot access a memory other than the one which it controls. In addition, Bass et al. does not teach or suggest buffer spread across multiple sector of the same memory element. As a consequence, Claim 34 is not anticipated by Bass et al.

C. Claims 24 and 27 are Not Obvious

C(1). Rejection of Claim 24

Claim 24 is rejected under 35 USC 103(a) as being obvious over U.S. Patent 6,450,227 (Bartoldus et al.) in view of Bass et al. It seems the Examiner relied on Bartoldus et al. for teaching the first three elements of Appellants' Claim 24 and on Bass et al for teaching the last element.

C(2). The Law As Applied To Rejection Under 35 USC 103(a)

(Obviousness)

In order to sustain a rejection of a claim under 35 USC 103(a), a prima facie case of obviousness has to be established. To do so, the prior art references when combined must teach or suggest all the limitations in the rejected claim. MPEP 2142.

C(3). Bass et al. Does Not Teach Or Suggest Limitations In Claim 24

Claim 24 calls for a single arbiter, in response to a request, causes different ones of the plurality of memory elements to be read simultaneously so that each one of the adjoining parts of the frame is available simultaneously over separate buss associated with each of the different ones of the plurality of memory elements.

As argued above and incorporated herein by reference, this feature of Appellants' claim is not found in Bass et al.

Bass et al. teaches multiple arbiter with each one associated with a single memory element. Fig. 13, Col. 24, lines 36-67. Bass et al. does not teach the simultaneous reading of separate memory element, or simultaneous availability of data on separate bus or a single arbiter enabling these functions. As a consequence even after the Examiner's combination, the resulting reference would not teach these features of Claim 24. Therefore, a prima facie case of obviousness has not been established and Claim 24 is not obvious in view of the references.

In discussing Bass et al. reference relative to the rejection of Claim 24, the Examiner at page 9 of the Final Office Action, mailed 08/24/2005 states: "Bass et al. further teaches that the memories are logically divided into sub-memories and that these submemories can be logically accessed simultaneously."

Appellants would like to point out that this quote relates to a single memory such as a DDRAM partitioned into four (4) banks. (Bass et al., Col. 25, lines 16-18.) This teaching has no relevancy to the "simultaneous" limitation of Claim 24 set forth above. In Claim 24, the simultaneous reading occurs on different ones of the plurality of separate memory storing different parts of the same frame and not on different banks in the same memory elements. As a consequence, the simultaneous limitation in Claim 24 is not suggested in Bass et al.

C(4). Novel Structure and Benefits Indicia of Unobviousness

As argued above and incorporated by reference, the structure of Claim 24 is novel. In particular, neither of the references Bartoldus et al. or Bass et al. teaches a single arbiter performing the functions recited in Claim 24. As a consequence, the structure of the claim is novel. The benefit provided by the claimed invention is a low cost high density memory system. Appellants' specification, page 2, lines 17-19; page 4, lines 4-7 and page 24, lines 4-7.

It is Appellants' contention the novel structure and benefits are indicia of unobviousness. Therefore, Claim 24 is patentable and not obvious in view of the references.

C(5). Rejection of Claim 27

Claim 27 is rejected under 35 USC 103(a) as being obvious over Bartoldus et al. (U.S. Patent 6,560,227) in view of Bass et al. (U.S. Patent 6,460,120) and Applicants' Admitted Prior Art (AAPA).

C(6). Limitation of Claim 27 Not Found in Reference

As to this rejection, Appellants contend a prima facie case of obviousness has not been established as is required to sustain this rejection (See C2 above).

In particular, the references when combined do not teach "simultaneously accessing, with a single arbiter, multiple ones of a plurality of separate memory modules in a single memory access window to read data therefrom wherein total bandwidth of data from the multiple memory modules matches the bandwidth of the FAT pipe."

Because the references do not teach this step of the claimed method, a prima facie case of obviousness has not been established. Therefore, Claim 27 is not obvious in view of cited references.

In addition, the method is novel and includes benefits set forth in C4 above and incorporated herein by reference. It has been held novel process and benefits are indicia of unobviousness. As a consequence, Claim 27 is patentable and not obvious in view of the references.

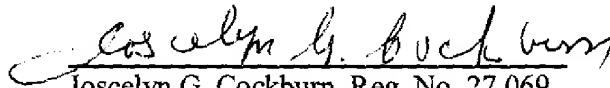
CONCLUSION

Based upon the above arguments, Bass et al. reference should be withdrawn. If it is the rejections under 35 USC 102(e) (anticipation) and 35 USC 103(a) (obviousness) must fall.

In the event Bass et al. is deemed applicable, Claims 1-4, 24-27, 33, and 34 (appealed claims) define patentable subject matter and are not anticipated or obvious by the cited art. As a consequence, the final rejection of these claims should be reversed.

Note: For convenience of detachment without disturbing the integrity of the remainder of pages of this Appeal Brief, Appellants' "APPENDIX" section is provided on separate sheets following the signatory portion of this Appeal Brief.

Respectfully Submitted,



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CLAIMS APPENDIX

1. A system comprising:
 - N different memories wherein $N > 1$;
 - M different busses with each one of the M different busses having a bandwidth to transport data at a predetermined rate, operatively coupled to each one of the N memories wherein M is greater than 1;
 - a plurality of different memory controllers with each one of the plurality of different memory controllers operatively coupled to one of the N memories, wherein said each one of the plurality of memory controllers setting an associated different memory in at least a first mode; and
 - a single arbiter responsive to at least one signal requesting access to the N different memories wherein said single arbiter generates an Access vector that causes information to be read simultaneously from multiple ones of the N different memories set in the at least a first mode wherein total bandwidth on selected ones of the M different busses of the N different memories is greater than the bandwidth on a single bus of the M different busses of the N different memories.
2. The system of Claim 1 wherein the at least first mode includes a Read mode.
3. The system of claims 1 or 2 wherein each of the N different memories includes DDR DRAM.
4. The system of claim 3 wherein each of the DDR DRAM is partitioned into at least four banks and at least one buffer is spread across the at least four banks.
24. A method comprising:
 - providing a plurality of separate memory elements in which frames from communication device are to be stored or retrieved;
 - partitioning at least one of the frames with a controller into at least two parts;

storing each one of the at least two parts into different ones of the plurality of separate memory elements; and

providing a single arbiter responsive to a request signal to cause the different ones of the plurality of separate memory elements to be read simultaneously wherein each one of the adjoining parts is available simultaneously on respective busses associated with each of said ones of the plurality of separate memory elements.

25. A method including:

providing a plurality of separate memories in which data is stored;

providing a single arbiter to grant access to the plurality of separate memories;

receiving in the single arbiter a request to read data from selected ones of said plurality of separate memories; and

simultaneously reading said selected ones of said plurality of separate memories to provide data simultaneously on individual busses coupled to the selected ones of said plurality of separate memories.

26. The method of claim 25 wherein the bandwidth of data on each one of the individual busses is less than the total bandwidth on all activated busses.

27. A method comprising:

providing a plurality of separate memory modules in which frames are being stored;

partitioning a frame into multiple parts;

writing adjacent parts of the frame so partitioned in different ones of the plurality of separate memory modules; and

simultaneously accessing, with a single arbiter, multiple ones of the plurality of separate memory modules in a single memory access window to read data therefrom wherein the total bandwidth of data output from the multiple memory modules matches the bandwidth of a FAT pipe port associated with a communication device.

33. A system comprising:

N different memory elements, $N > 1$, wherein at least two of said N different memory elements are each partitioned into multiple sectors and each of the at least two of said N different memory elements so partitioned is partitioned into at least one buffer spread across said multiple sectors;

a plurality of memory controllers with each one of said plurality of memory controllers operatively coupled to each one of the N different memory elements; and

a single arbiter operatively coupled to the plurality of memory controllers, said single arbiter being responsive to a write request signal to generate a write control signal that causes data to be written in one of the at least one buffer associated with one of the at least two of said N different memory elements.

34. The system of claim 33 further including said single arbiter being responsive to a read request signal to generate a read control signal that causes data to be read from another of the at least one buffer associated with another of the at least two of said N different memory elements.

EVIDENCE APPENDIX

This appendix contains Declaration under 37 CFR 1.132 filed by Appellants and admitted into evidence by Examiner.

In addition, page 700-250 of the MPEP providing legal support for sufficiency of Appellants' Declaration under 37 CFR 1.132 is also included.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings to the current appeal.